IN THE CLAIMS:

Please amend claims 1-3 and 39-41 as follows.

1. (Currently Amended) A method, comprising:

determining, at a processor, a limiting signal from a transmissible signal filtered using a pulse shaping filter;

determining an error signal using the transmissible signal and the limiting signal; and

generating a limited transmissible signal by reducing an error signal filtered using the filter matched to a chip pulse waveform from the transmissible signal.

2. (Currently Amended) A method, comprising:

determining, at a processor, a limiting signal from a transmissible signal filtered using a pulse shaping filter;

determining an error signal using the transmissible signal and the limiting signal;

orthogonalizing the error signal filtered using the filter matched to a chip pulse waveform; and

generating a limited transmissible signal by reducing the orthogonalized error signal from the transmissible signal.

3. (Currently Amended) A method, comprising:

combining, at a processor, at least two signals modulated on different carriers to a combination signal;

determining a limiting signal from the combination signal filtered using a pulse shaping filter;

determining an error signal using the combination signal and the limiting signal;

dividing the error signal onto different carriers in a predetermined manner; and

generating limited transmissible signals by reducing each error signal part filtered using the filter matched to a chip pulse waveform from a corresponding transmissible signal.

4. (Previously Presented) The method as claimed in claim 1, wherein the transmissible signal is a baseband signal.

5. (Previously Presented) The method as claimed in claim 1, wherein the limiting signal is a baseband signal.

6. (Previously Presented) The method as claimed in claim 1, wherein the error signal is a baseband signal.

7. (Previously Presented) The method as claimed in claim 1, wherein the limiting signal is determined using a threshold value set for power or amplitude values.

8. (Previously Presented) The method as claimed in claim 1, wherein the limiting signal is determined using a threshold value set for power or amplitude values, the threshold value being set bearing in mind the maximum value predetermined for an error vector magnitude.

9. (Previously Presented) The method as claimed in claim 1, wherein the limiting signal is determined using a threshold value set for power or amplitude values, the threshold value being set bearing in mind the maximum value predetermined for a peak code domain error.

10. (Previously Presented) The method as claimed in claim 1, wherein the limiting signal is determined using a threshold value set for power or amplitude values, the threshold value being set so as to obtain the desired peak-to-mean ratio, peak-to-average ratio, crest factor of the power or amplitude.

11. (Previously Presented) The method as claimed in claim 2, wherein a second clipping stage is added.

12. (Previously Presented) The method as claimed in claim 2, wherein orthogonalization is carried out by minimizing the equation

$$\left| \begin{bmatrix} x_1 & x_2 & \cdots & x_p \end{bmatrix} \begin{bmatrix} c_{1,1} & c_{2,1} & \cdots & c_{n,1} \\ c_{1,2} & c_{2,2} & \ddots & c_{n,2} \\ \vdots & \vdots & \ddots & \vdots \\ c_{1,p} & c_{2,p} & \cdots & c_{n,p} \end{bmatrix} - \begin{bmatrix} y_1 & y_2 & \cdots & y_n \end{bmatrix} \right|.$$

13. (Previously Presented) The method as claimed in claim 2, wherein unused codes are utilized in orthogonalization.

14. (Previously Presented) The method as claimed in claim 2, wherein codes used at a lower modulation level are utilized in orthogonalization.

15. (Previously Presented) The method as claimed in claim 3, wherein the orthogonalization of the error signal is carried out according to carriers.

16. (Previously Presented) The method as claimed in claim 3, wherein the error signal is divided equally between different carriers.

17. (Previously Presented) The method as claimed in claim 3, wherein the error signal is divided between different carriers in relation to power or amplitude values to be clipped.

18. (Previously Presented) An apparatus, comprising:

means for determining a limiting signal from a transmissible signal filtered using a pulse shaping filter;

means for determining an error signal using the transmissible signal and the limiting signal;

means for generating a limited transmissible signal by reducing the error signal filtered using the filter matched to a chip pulse waveform from the transmissible signal; and

means for filtering the limited transmissible signal using the pulse shaping filter.

19. (Previously Presented) An apparatus, comprising:

means for determining a first limiting signal from a transmissible signal filtered using a pulse shaping filter;

means for determining a first error signal using the transmissible signal and the first limiting signal;

means for orthogonalizing the first error signal filtered using the filter matched to a chip pulse waveform;

means for generating a first limited transmissible signal by reducing the orthogonalized first error signal from the transmissible signal;

means for determining a second limiting signal from the first limited transmissible signal filtered using the pulse shaping filter;

means for determining a second error signal using the first limited transmissible signal and the second limiting signal;

means for generating a second limited transmissible signal by reducing the second error signal filtered using the filter matched to a chip pulse waveform from the transmissible signal; and

means for filtering the second limited transmissible signal using the pulse shaping filter.

20. (Previously Presented) An apparatus, comprising:

means for combining at least two signals modulated on different carriers to a combination signal;

means for determining a limiting signal from the combination signal filtered using a pulse shaping filter;

means for determining an error signal using the combination signal and the limiting signal;

means for dividing the error signal onto different carriers in a predetermined manner;

means for generating limited transmissible signals by reducing each error signal part filtered using the filter matched to a chip pulse waveform from a corresponding transmissible signal;

means for filtering the limited transmissible signals using the pulse shaping filter; and

means for generating a combined limited transmissible signal by combining the filtered limited transmissible signals.

21. (Previously Presented) An apparatus, comprising:

means for filtering transmissible signals modulated on different carriers using pulse shaping filters;

means for combining at least two filtered signals to a combination signal;

means for determining a limiting signal from the combination signal;

means for determining an error signal using the combination signal and the limiting signal;

means for dividing the error signal onto different carriers in a predetermined manner;

means for generating limited transmissible signals by reducing each error signal part filtered using the filter matched to a chip pulse waveform from a corresponding transmissible signal;

means for filtering the limited transmissible signals using the pulse shaping filter; and

means for generating a combined limited transmissible signal by combining the filtered limited transmissible signals.

22. (Previously Presented) The apparatus as claimed in claim 35, wherein the transmissible signal is a baseband signal.

23. (Previously Presented) The apparatus as claimed in claim 35, wherein the limiting signal is a baseband signal.

24. (Previously Presented) The apparatus as claimed in claim 35, wherein the error signal is a baseband signal.

25. (Previously Presented) The apparatus as claimed in claim 35, wherein the limiting determiner is further configured to determine the limiting signal using a threshold value set for power or amplitude values.

26. (Previously Presented) The apparatus as claimed in claim 35, wherein the limiting determiner is further configured to determine the limiting signal using a

threshold value set for power or amplitude values, the threshold value being set bearing in mind the maximum value predetermined for an error vector magnitude.

27. (Previously Presented) The apparatus as claimed in claim 35, wherein the limiting determiner is further configured to determine the limiting signal using a threshold value set for power or amplitude values, the threshold value being set bearing in mind the maximum value predetermined for a peak code domain error.

28. (Previously Presented) The apparatus as claimed in claim 35, wherein the limiting determiner is further configured to determine the limiting signal using a threshold value set for power or amplitude values, the threshold value being set so as to obtain the desired peak-to-mean ratio, peak-to-average ratio, crest factor of the power or amplitude.

29. (Previously Presented) The apparatus as claimed in claim 36, wherein the processor is further configured to carry out the orthogonalization of the first error signal according to carriers.

30. (Previously Presented) The apparatus as claimed in claim 37, wherein the divider is further configured to divide the error signal equally between different carriers.

31. (Previously Presented) The apparatus as claimed in claim 37, wherein the divider is further configured to divide the error signal between different carriers in relation to power or amplitude values to be clipped.

32. (Previously Presented) The apparatus as claimed in claim 36, wherein the processor is further configured to carry out orthogonalization by minimizing the equation

$$\left| \begin{bmatrix} x_1 & x_2 & \cdots & x_p \end{bmatrix} \begin{bmatrix} c_{1,1} & c_{2,1} & \cdots & c_{n,1} \\ c_{1,2} & c_{2,2} & \ddots & c_{n,2} \\ \vdots & \vdots & \ddots & \vdots \\ c_{1,p} & c_{2,p} & \cdots & c_{n,p} \end{bmatrix} - \begin{bmatrix} y_1 & y_2 & \cdots & y_n \end{bmatrix} \right|.$$

33. (Previously Presented) The apparatus as claimed in claim 36, wherein the processor is further configured to carry out orthogonalization utilizing unused codes.

34. (Previously Presented) The apparatus as claimed in claim 36, wherein the processor is further configured to carry out orthogonalization utilizing codes used at a lower modulation level.

35. (Previously Presented) An apparatus, comprising:

a limiting determiner configured to determine a limiting signal from a transmissible signal filtered using a pulse shaping filter;

an error determiner configured to determine an error signal using the transmissible signal and the limiting signal;

a generator configured to generate a limited transmissible signal by reducing the error signal filtered using the filter matched to a chip pulse waveform from the transmissible signal; and

a filter configured to filter the limited transmissible signal using the pulse shaping filter.

36. (Previously Presented) An apparatus, comprising:

a first limiting determiner configured to determine a first limiting signal from a transmissible signal filtered using a pulse shaping filter;

a first error determiner configured to determine a first error signal using the transmissible signal and the first limiting signal;

a processor configured to orthogonalize the first error signal filtered using the filter matched to a chip pulse waveform;

a first generator configured to generate a first limited transmissible signal by reducing the orthogonalized first error signal from the transmissible signal;

a second limiting determiner configured to determine a second limiting signal from the first limited transmissible signal filtered using the pulse shaping filter;

a second error determiner configured to determine a second error signal using the first limited transmissible signal and the second limiting signal;

a second generator configured to generate a second limited transmissible signal by reducing the second error signal filtered using the filter matched to a chip pulse waveform from the transmissible signal; and

a filter configured to filter the second limited transmissible signal using the pulse shaping filter.

37. (Previously Presented) An apparatus, comprising:

a combiner configured to combine at least two signals modulated on different carriers to a combination signal;

a limiting determiner configured to determine a limiting signal from the combination signal filtered using a pulse shaping filter;

an error determiner configured to determine an error signal using the combination signal and the limiting signal;

a divider configured to divide the error signal onto different carriers in a predetermined manner;

a first generator configured to generate limited transmissible signals by reducing each error signal part filtered using the filter matched to a chip pulse waveform from a corresponding transmissible signal;

a filter configured to filter the limited transmissible signals using the pulse shaping filter; and

a second generator configured to generate a combined limited transmissible signal by combining the filtered limited transmissible signals.

38. (Previously Presented) An apparatus, comprising:

a filter configured to filter transmissible signals modulated on different carriers using pulse shaping filters;

a combiner configured to combine at least two filtered signals to a combination signal;

a limiting determiner configured to determine a limiting signal from the combination signal;

an error determiner configured to determine an error signal using the combination signal and the limiting signal;

a divider configured to divide the error signal onto different carriers in a predetermined manner;

a first generator configured to generate limited transmissible signals by reducing each error signal part filtered using the filter matched to a chip pulse waveform from a corresponding transmissible signal;

a filter configured to filter the limited transmissible signals using the pulse shaping filter; and

a second generator configured to generate a combined limited transmissible signal by combining the filtered limited transmissible signals.

39. (Currently Amended) ~~A computer program, embodied on a computer-readable medium,~~ A computer-readable medium encoded with a computer program, for controlling a processor to implement a method, the method comprising:

determining a limiting signal from a transmissible signal filtered using a pulse shaping filter;

determining an error signal using the transmissible signal and the limiting signal; and

generating a limited transmissible signal by reducing an error signal filtered using the filter matched to a chip pulse waveform from the transmissible signal.

40. (Currently Amended) ~~A computer program, embodied on a computer-readable medium,~~ A computer-readable medium encoded with a computer program, for controlling a processor to implement a method, the method comprising:

determining a limiting signal from a transmissible signal filtered using a pulse shaping filter;

determining an error signal using the transmissible signal and the limiting signal;

orthogonalizing the error signal filtered using the filter matched to a chip pulse waveform; and

generating a limited transmissible signal by reducing the orthogonalized error signal from the transmissible signal.

41. (Currently Amended) ~~A computer program, embodied on a computer-readable medium,~~ A computer-readable medium encoded with a computer program, for controlling a processor to implement a method, the method comprising:

combining at least two signals modulated on different carriers to a combination signal;

determining a limiting signal from the combination signal filtered using a pulse shaping filter;

determining an error signal using the combination signal and the limiting signal;

dividing the error signal onto different carriers in a predetermined manner; and

generating limited transmissible signals by reducing each error signal part filtered using the filter matched to a chip pulse waveform from a corresponding transmissible signal.